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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,818	ELDRIDGE ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 85-95* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16,17,19 and 87-95* is/are allowed.

6)☒ Claim(s) *1-15,18,20-23,85 and 86* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) __ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's Amendment filed 08/02/2005 has been reviewed and placed of record in the file.

Claim Rejections - 35 USC § 102 or 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claim 1, 3, 4, and 9** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Endo U.S. Patent 5,619,051 (the '051 patent, cited in a previous office action).

Referring to **claim 1**, the reference discloses a floating gate transistor, comprising:

a first source/drain region (22 or 24, Fig. 5) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate (10);

a floating gate (16) opposing the channel region and separated therefrom by a gate oxide (14);

a control gate (20) opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator (18A, wherein "the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane", column 7, lines 1-8, and where "low" is interpreted broadly, and where the "tunnel barrier" property is

interpreted to be inherent as the stepwise-graded dielectric layer 18A is a barrier to, for example, electrons tunneling from, for example, from the floating gate to, for example, the control gate).

However, the reference does not explicitly and positively disclose the limitation "asymmetrical" for the low tunnel barrier intergate insulator, and the low tunnel barrier intergate insulator 18A is formed by a CVD (deposition) process rather than by multiple ALD deposition process as claimed.

Nevertheless, as for the limitation "asymmetrical", the reference discloses that, as noted above, proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane. In other words, at least the portion of the lower surface and the portion of the upper surface of the low tunnel barrier intergate insulator 18A are formed of different mixtures of different metal oxides, thus having different barrier heights, thus meeting the definition of "asymmetrical". See also column 7, last paragraph for a description of a 0.4eV difference in barrier heights between the two surfaces.

As for the limitation CVD as disclosed by the reference and the claimed multiple ALD, since the two processes both appear to result in an asymmetrical low tunnel barrier intergate insulator, the asymmetrical low tunnel barrier intergate insulator formed by multiple ALD is not patently distinguishable from the asymmetrical low tunnel barrier intergate insulator formed by CVD. In addition, according to another doctrine, a process limitation, such as ALD, is considered a non-limitation in a product claim, if, as, or since the process does not result in a difference in structure, a device having an asymmetrical low tunnel barrier intergate insulator in the instant case, as compared to prior art.

Referring to **claim 3**, the reference further discloses that that asymmetrical low tunnel barrier intergate insulator includes an asymmetrical transition metal oxide, as $SrTiO_3$ (column 7, lines 9-12) is a transition metal oxide.

Referring to **claim 4**, although the reference's transition metal oxide is formed of a transition metal not the same as one of the claimed transition metals, they are all transition metals, therefore their metal oxides should be functionally equivalent.

Referring to **claim 9**, although the reference does not explicitly discloses that the floating gate transistor is an n-channel type floating gate transistor, one of ordinary skill in the art recognizes that an n-channel type floating gate transistor and a p-channel type floating gate transistor are only different in the dopants (n or p) used.

3. **Claims 10, 11, 14, and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) in view of Orlowski et al. U.S. Patent 6,433,382.

Referring to **claim 10**, the '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claim 1 including the asymmetrical low tunnel barrier intergate insulator 18A and a first source/drain region (22 or 24) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator has a number of small compositional ranges ("the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane", column 7, lines 1-8). However, the

reference fails to disclose a body region including the channel region and that the body region including the channel region is formed on the first source/drain region. In other words, the reference discloses a "planar" non volatile memory cell instead of a vertical non volatile memory cell as claimed.

Orlowski, in disclosing also a non volatile memory cell including a pair of source/drain regions, a channel region, a floating gate, and a control gate, teaches that vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, reduced masking steps, and fully inverted or fully depleted channel regions (column 14, first paragraph). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's non volatile memory cell such that it has a vertical configuration. One would have been motivated to make such a change because a vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, reduced masking steps, and fully inverted or fully depleted channel regions, as taught by Orlowski.

Referring to **claim 11**, the '051 patent's material ($SrTiO_3$, column 7, lines 9-12) for the asymmetrical low tunnel barrier intergate insulator meets the limitation of the claimed Markush group of materials.

Referring to **claims 14 and 15**, the device of the '051 patent modified in view of Orlowski thus comprises a vertical floating gate (such as 30, Orlowski's Fig. 1 or Fig. 10) along side a body region (22 or 58), and a vertical control gate (32) along side the vertical floating gate.

4. **Claims 5 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) as applied to claim 1 above, and further in view of Eguchi et al. U.S. Patent 5,618,761.

The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above including the asymmetrical low tunnel barrier intergate insulator 18A. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator is formed of $SrTiO_3$ (column 7, lines 9-12) by a CVD process, meeting the limitation of the claimed Markush group of materials of claim 6. The reference further discloses that the asymmetrical low tunnel barrier intergate insulator ought to have a high dielectric constant (the table in column 6, lines 35-45, and claim 1). However, the reference fails to mention the limitation "Perovskite" for the asymmetrical low tunnel barrier intergate insulator.

Eguchi, in disclosing an insulator layer for a capacitor, mentions that a layer comprising Sr, Ti, and O formed by CVD process, has a perovskite crystal structure, which offers a high dielectric constant and excellent insulating properties (column 9, lines 37-45). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '051 patent's asymmetrical oxide tunnel barrier intergate insulator such that it is an asymmetrical Perovskite oxide tunnel barrier intergate insulator. One would have been motivated to make such a change because perovskite crystal structure offers a high dielectric constant and excellent insulating properties, which high dielectric constant property is desired by the '051 patent and which is taught by Eguchi.

5. **Claims 7-8, 12-13, and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent).

The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1 and 10 including the asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously of stepwise" from the bottom surface to the top surface. The reference further discloses, in reference to **claim 18**, that the number of small compositional ranges is formed such that gradients can be formed in an applied electric field which produce different barrier heights at an interface with the floating gate and control gate (paragraph bridging columns 7 and 8, particularly "...gradient of conduction band to make an about 0.4 eV difference...information charge retention time is about twice that in the memory cell of FIG. 1...the erase time shortens to 1/5 of that in the memory cell having the dielectric film 18 of homogeneous barium strontium titanate).

The reference further teaches that the floating gate includes a polysilicon floating gate having a metal silicide formed thereon (column 3, lines 56-63) in contact with the asymmetrical low tunnel barrier intergate insulator, and that the control gate includes a metal control gate having a metal oxide layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

Compared with the claims, the reference discloses a metal silicide instead of the claimed first metal layer for the floating gate, a metal oxide/metal instead of the claimed second metal/polysilicon for the control gate. However, the differences are deemed to be obvious to one of ordinary skill in the art at the time the invention was made ("the artisan") because at least one

of the following two reasons: (1) the materials are known and available to the artisan; (2) both the present invention and the reference fails to show an advantage of one combination of materials to the other.

With respect to the limitation "wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate", the limitation appears to be inherent in the reference because: (1) the metal of the metal silicide (functionally equivalent to the claimed first metal) and the metal of the metal oxide (functionally equivalent to the claimed second metal) are different metals, resulting in different work functions; (2) the paragraph bridging columns 7 and 8, as noted above, expressly states that the barrier heights at the two surfaces of the asymmetrical low tunnel barrier intergate insulator, where the metal silicide and the metal oxide are respectively in contact with, ought to be different, leading the artisan to conclude that the work function of the metal silicide (functionally equivalent to the claimed first metal) should be different from the work function of the metal oxide (functionally equivalent to the claimed second metal).

6. **Claim 23** is rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) as applied above for claim 18 and further in view of Orlowski et al. U.S. Patent 6,433,382.

Similarly as detailed above for claims 10, 11, 14, and 15, the artisan would be motivated to forms the floating gate transistor such that it includes a vertical floating gate transistor.

7. **Claims 2, 20-22, and 85-86** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) in view of Shinkawata et al. U.S. Patent Application Publication 20020008324.

The '051 patent discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1, 6, 10, and 18 including the asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously of stepwise" from the bottom surface to the top surface, and wherein the number of small compositional ranges arranged in a "vary continuously of stepwise" includes $SrTiO_3$ (column 7, lines 1-12). The materials for the second metal (in reference to claims 20 and 21) should also be known and available to the artisan as noted above.

However, instead of the claimed aluminum oxide (Al_2O_3), as noted, the reference discloses $SrTiO_3$.

Shinkawata, in disclosing a gate insulating film 24 for semiconductor device, teaches that the two materials are equivalent (paragraph [0063]) (and they should be because otherwise the claimed device of claims 6, 11, 20-22, which contains both materials, would be inoperable).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '051 patent's asymmetrical low tunnel barrier intergate insulator such that it includes aluminum oxide (Al_2O_3) instead of $SrTiO_3$. One would certainly be motivated to do that as a choice of available and equivalent materials.

Response to Arguments

8. Applicant's arguments with respect to claims 1-15, 17-18, 20-23, and 85-86, filed 08/02/2005, have been fully considered but they are not persuasive.

With respect to Applicant's arguments on page 10 that the '051 patent does not disclose a difference in barrier heights between the two surfaces, it is respectfully pointed out that the '051 patent discloses a difference in barrier heights between the two surfaces. Specifically, the reference discloses in columns 1-10, particularly columns 7-8, more particularly the paragraph bridging columns 7 and 8, that the forbidden band width of the intergate insulator barrier 18a at the interface with the floating gate 16 is about 3.0eV and that at the interface with control gate 20 is about 3.4 eV (column 7, lines 55+). While it is true that a forbidden band width is not the same as a barrier height, it is known that in the case of non-metal, specifically in the case of metal oxide non-metal, more particular in the case of an intergate insulator as in the present situation, the barrier height (Fermi level) value lies within the forbidden band width, and this barrier height is dependent upon the characteristics of the materials of the intergate insulator. As the material of the reference's intergate insulator is formed "of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously of stepwise from the bottom plane adjacent to the floating gate 16 to the top plane" (column 7, lines 1-8, emphasis added by the examiner), the Fermi level, or the barrier height, shall correspond to the forbidden band: when the forbidden band (value) is narrower (lower), the barrier height is lower, and when the forbidden band (value) is wider (higher), the barrier height is higher. Therefore, although not in so many words, the '051 patent discloses a difference in barrier heights between the two surfaces.

As for the limitation "formed by multiple atomic layer deposition (ALD)", again, the limitation is a product-by-process limitation, and a product-by-process limitation in a device claim is evaluated only to the extent to which it applies to the claimed device, which is a device having an asymmetrical low tunnel barrier intergate insulator as in the instant case, which is also disclosed by the '051 patent, as detailed thus far.

Allowable Subject Matter

9. Claims 16-17, 19, and 87-95 are allowable over the prior art of record.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a non-volatile memory cell having all exclusive limitations as recited in claims 16 and 19, characterized in the limitations of claims 16 and 19 respectively.

Conclusion

10. THIS ACTION IS MADE FINAL. **Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).**

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
September 21, 2005